REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, claims 2 and 5 have been amended, and new claims 7-9 added. Claims 1 and 4 were previously withdrawn from consideration. Thus, claims 2-3 and 5-9 are currently pending in the application and subject to examination.

In the Office Action mailed May 31, 2006, the Examiner rejected claims 2 and 5 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,438,665 to Taniai et al. ("Taniai"). The Examiner rejected claims 3 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Taniai in view of U.S. Patent No. 5,640,598 to Sato et al. ("Sato") and further in view of JP 02195464 to Hoshino ("Hoshino").

Claims 2, 5, and 7-9

The Applicants' invention as now set forth in amended claim 2 is directed to a DMA controller including an operation counter for performing counting operation by use of data stored in a first register; an operation controller for performing control so that, when DMA transfer is started, an occurrence of data storage in the first register is counted by the operation counter; and a transfer executer for executing DMA transfer based on the operation counter.

This allows information for DMA transfer from a CPU to be stored in a first register and the DMA transfer to be executed according to the values in a group of counters. Thus, it is possible to make settings for DMA transfer even on a DMA channel that is currently being used. Even if all DMA channels are being used, it is possible to make settings for a DMA transfer without waiting for the end of the current

DMA transfer, which reduces wasted processing time in the CPU resulting from task switching.

Taniai teaches a DMAC including a transfer control circuit 22 and a transfer execution circuit 23. In the Office Action, the Examiner asserted that Taniai teaches the previously claimed "an operation register (see item 24 in figure 2) . . . , or an operation counter . . . (see lines 6-33 of column 4)." Column 4, lines 6-33 of Tanai, however, does not teach an operation counter. Thus, the Applicants submit that Taniai does not disclose or suggest at least an operation counter for performing counting operation by use of the data stored in a first register, as presently claimed in claim 2.

For at least this reason, the Applicants submit that claim 2 is allowable over the cited art. For similar reasons, the Applicants submit that claim 5 is likewise allowable. As claim 2 is allowable, the Applicants submit that newly added claims 7-9, which depend from allowable claim 2, are also allowable for at least the above noted reason and for the additional limitations they provide.

Claims 3 and 6

The Applicants' invention as set forth in claim 3 is directed to a DMA controller including an operation register for storing transfer conditions under which DMA transfer is currently being executed; a selector for alternatively selecting one of the setting register and the setting execution register; and an operation register controller for performing control so that, when DMA transfer is started, data stored in the register selected by a selector is written to the operation register.

The features of claim 3 allow a CPU to make settings for DMA transfer by writing transfer conditions to an external memory so that settings for a plurality of sessions of

DMA transfer can be made at one time. This reduces the amount of CPU processing time that is used to make settings for DMA transfer.

In the Office Action, the Examiner asserts that Taniai teaches an "operation register (see item 24 in figure 2) for permitting data stored in the setting register to be written thereto, or an operation counter for performing counting operation by use of the data (see lines 6-33 of column 4)." However, claim 3 recites "an operation register for storing transfer conditions under which DMA transfer is to be executed next time." Thus, the Applicants submit that Taniai does not disclose or suggest an operation register for storing transfer conditions under which DMA transfer is to be executed next time, as claimed in claim 3.

The Examiner also asserts that Taniai teaches an operation controller (element 22 in Taniai) for performing control so that, when DMA transfer is started, "the data stored in the setting register" is written to the operation register. In contrast, claim 3 includes an operation register controller for performing control so that, when DMA transfer is started, "data stored in the register selected by the selector" is written to the operation register. The Examiner previously indicated that element 22 was the "operation controller" in claims 2 and 5. Here, the Examiner indicates that the same element 22 is the "operation register controller" of claim 3. However, the Examiner describes the operation register controller with language that corresponds to the operation controller of claims 2 and 5 rather than the operation register controller of claim 3. Thus, the Applicants submit that element 22 is not the "operation register controller" that controls data stored in the register selected by the selector, as claimed in claim 3.

Sato and Hoshino fail to cure the deficiency in Taniai.

Furthermore, the Examiner relies on Hoshino as teaching a selector for alternatively selecting one of the setting register and the setting execution register and a selection controller for performing control so that the register selected by the selector is switched alternately between the setting register and the setting execution register every time DMA transfer ends.

Hoshino teaches DMA transfer setting conditions stored in register files 1 to 3. In each DMA transfer, transfer setting conditions from register file 1 are sent to an address counter, conditions from register file 2 are sent to a length counter, and setting conditions from register file 3 are sent to a more register. (See figure 2 and the abstract). After a DMA transfer, Hoshino teaches a selector that selects other set transfer conditions from register files 1 to 3 for another DMA transfer. However, Hoshino does not disclose or suggest at least a selector for alternatively selecting one of a setting register and a setting execution register. Instead, Hoshino teaches a selector for selecting set transfer conditions from the register files, where information from each of the register files is selected for each transfer.

For at least these reasons, the Applicants submit that claim 3 is allowable over the cited art. For similar reasons, the Applicants submit that claim 6 is likewise allowable.

With regard to each of the rejections under §103 in the Office Action, it is also respectfully submitted that the Examiner has not yet set forth a *prima facie* case of obviousness. The PTO has the burden under §103 to establish a *prima facie* case of obviousness. In re Fine, 5 U.S.P.Q.2nd 1596, 1598 (Fed. Cir. 1988). Both the case law

of the Federal Circuit and the PTO itself have made clear that where a modification must be made to the prior art to reject or invalidate a claim under §103, there must be a showing of proper motivation to do so. The mere fact that a prior art reference could arguably be modified to meet the claim is insufficient to establish obviousness. The PTO can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. See also In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984) (prior art could not be turned upside down without motivation to do so); In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998); In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Lee, 277 F.3d 1338 (Fed. Cir. 2002).

In the Office Action, the Examiner merely states that the present invention is obvious in light of the cited references. See, e.g., Office Action at page 3. This is an insufficient showing of motivation.

CONCLUSION

For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, with reference to Attorney Docket No. 103213-00057.

Respectfully submitted,

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